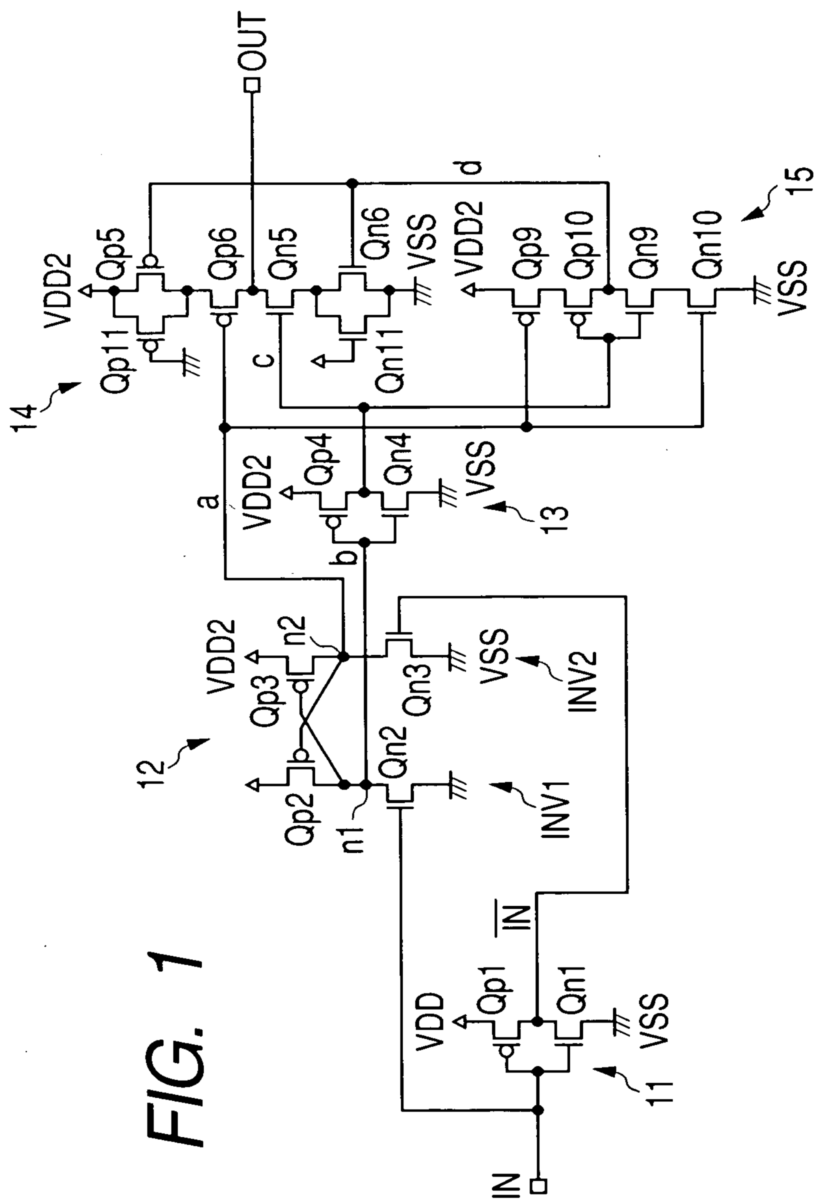

IN
11
VDD
Qp1
Qn1
VSS
IN
12
Qp2
Qp3
VDD2
n1
n2
Qn2
Qn3
VSS
INV1
INV2
a
b
VDD2
Qp4
Qn4
VSS
13
14
Qp11
Qp5
VDD2
Qp6
Qn5
c
Qn11
Qn6
VSS
OUT
d
VDD2
Qp9
Qp10
Qn9
Qn10
VSS
15

FIG. 1

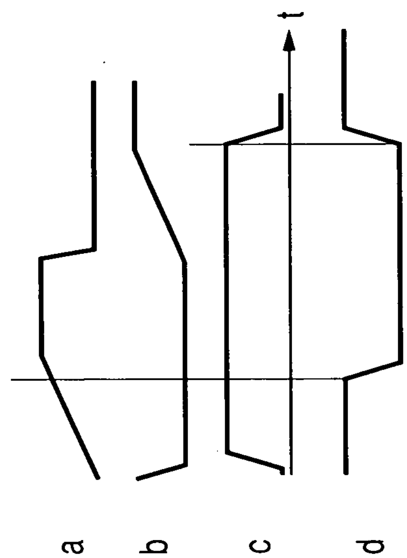

a
b
c
d
t

FIG. 2

FIG. 3(B)

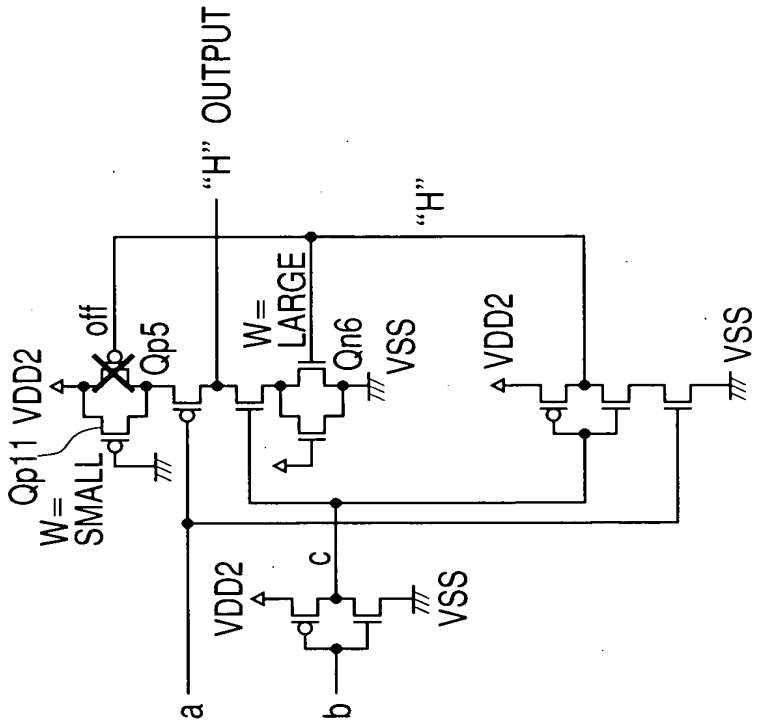


FIG. 3(A)

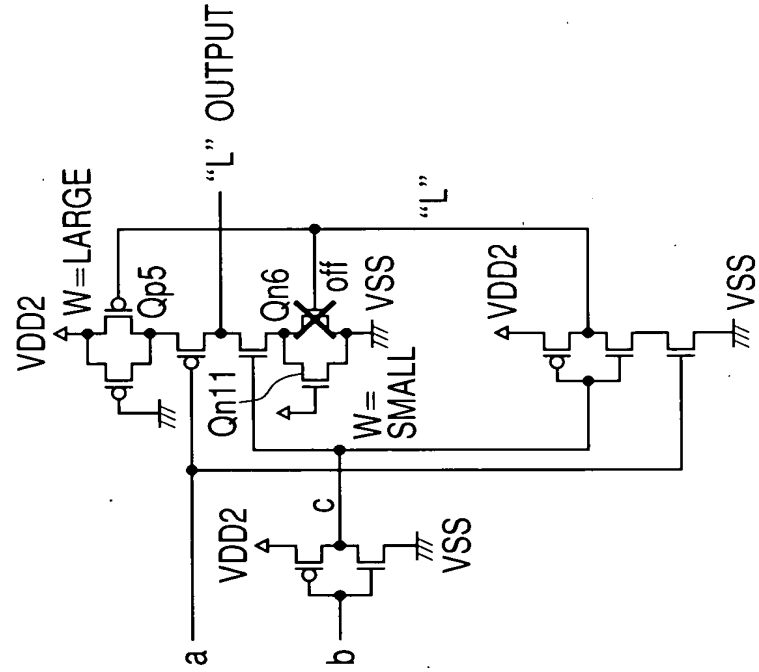
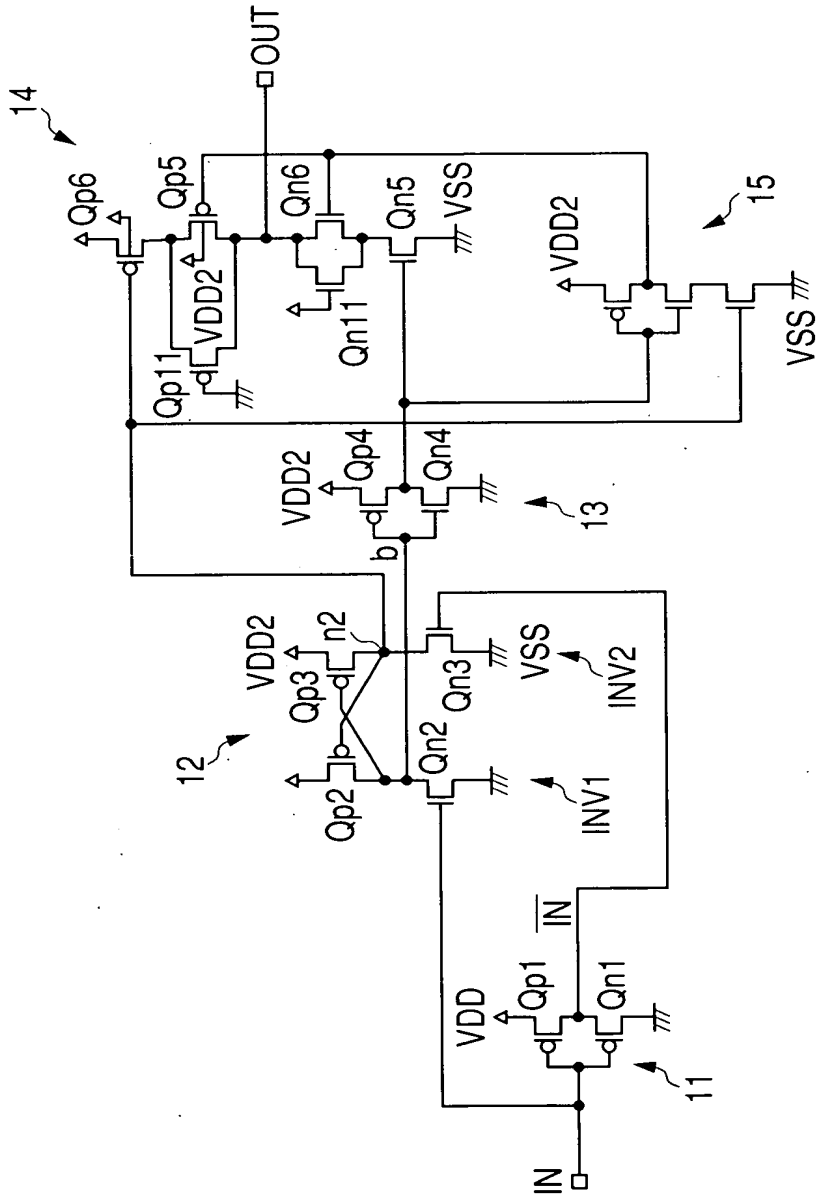


FIG. 4


OUT
14
Qp6
Qp5
Qn6
Qn5
VSS
VDD2
15
Qp11
VDD2
Qn11
VSS
VDD2
Qp4
Qn4
13
b
VDD2
Qp3
n2
Qn3
VSS
INV2
12
b
Qp2
Qn2
INV1
IN
VDD
Qp1
Qn1
11
IN

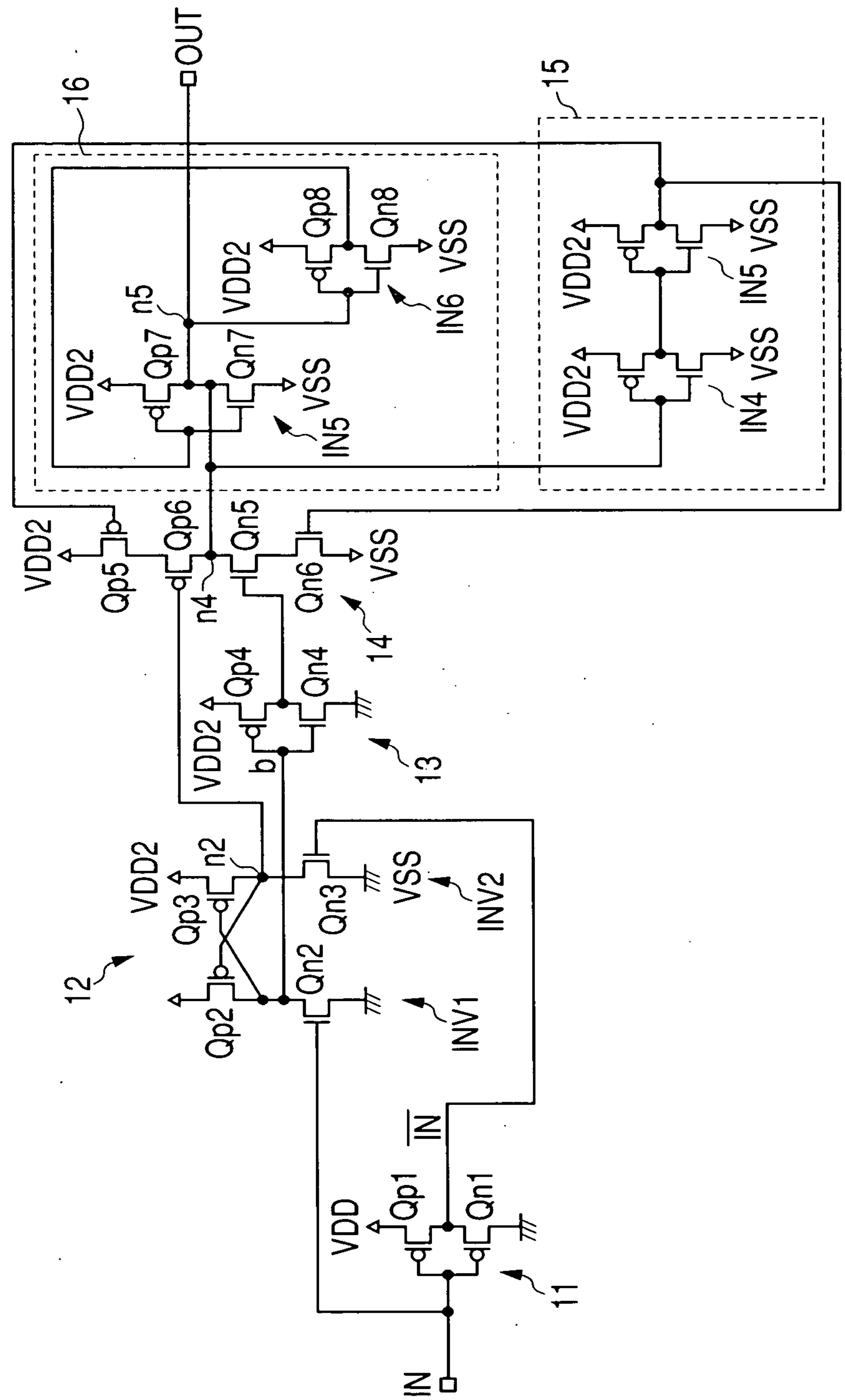

IN
VDD
Qp1
Qn1
11
IN
INV1
INV2
Qp2
Qn2
Qp3
Qn3
VDD2
VSS
n2
12
Qp4
Qn4
b
13
Qp5
Qp6
Qn5
Qn6
n4
14
VDD2
VSS
Qp7
Qn7
IN5
n5
Qp8
Qn8
IN6
16
OUT
IN4
IN5
15

FIG. 5

FIG. 6

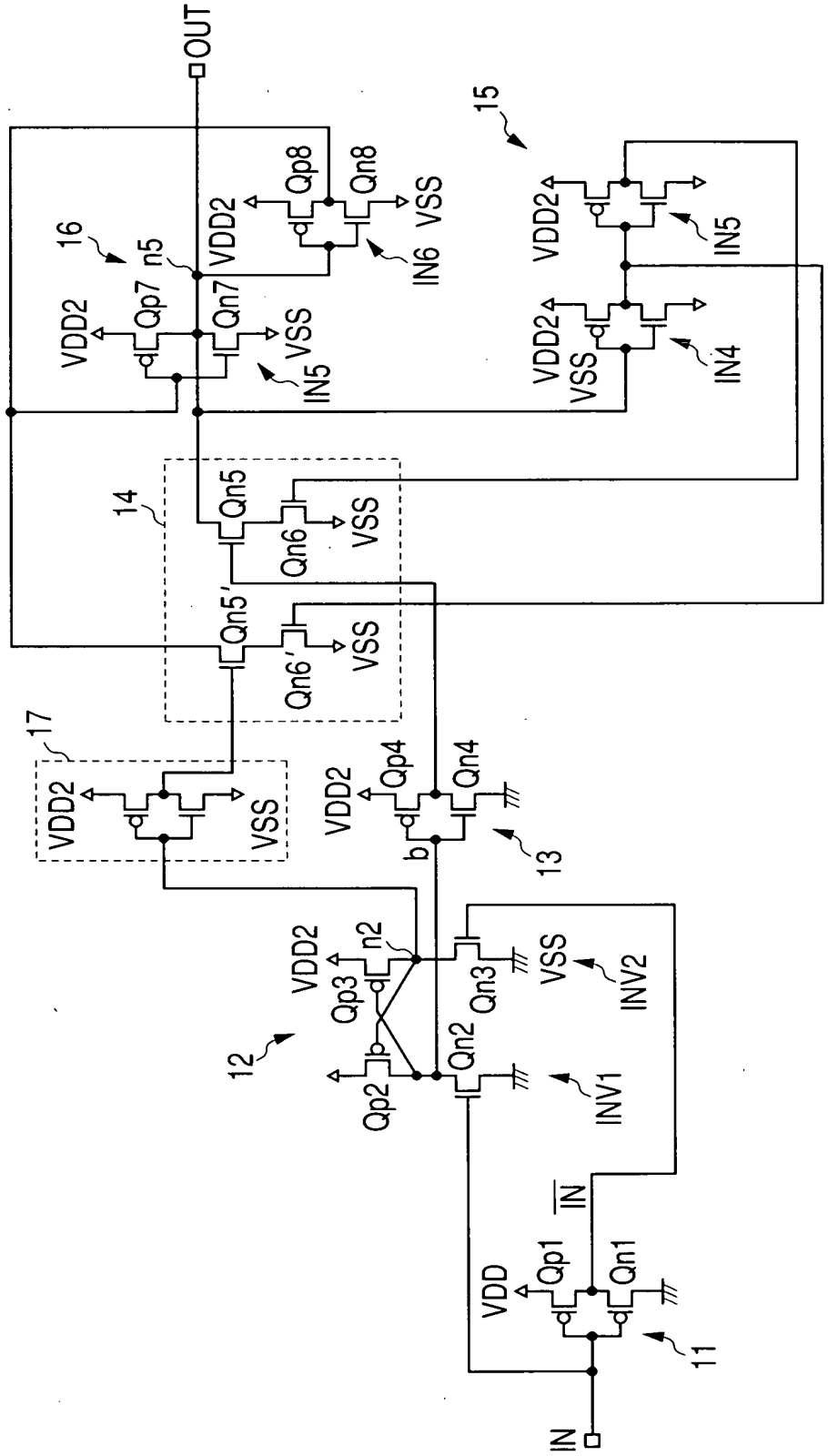


FIG. 7

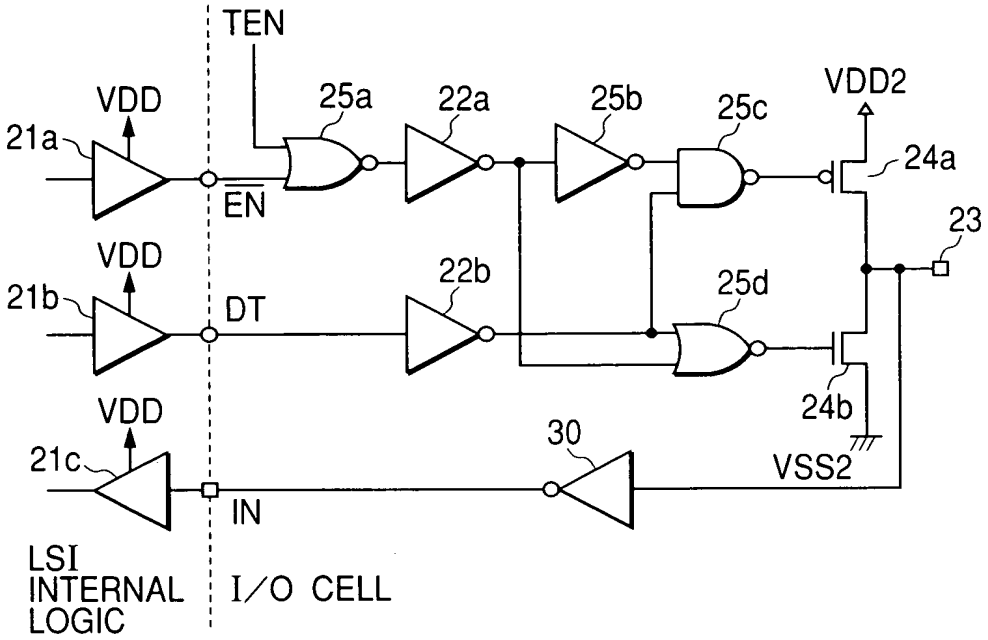

TEN
VDD
21a
25a
22a
25b
25c
VDD2
24a
EN
23
VDD
21b
DT
22b
25d
24b
VDD
21c
30
VSS2
IN
LSI
INTERNAL
LOGIC
I/O CELL

FIG. 8

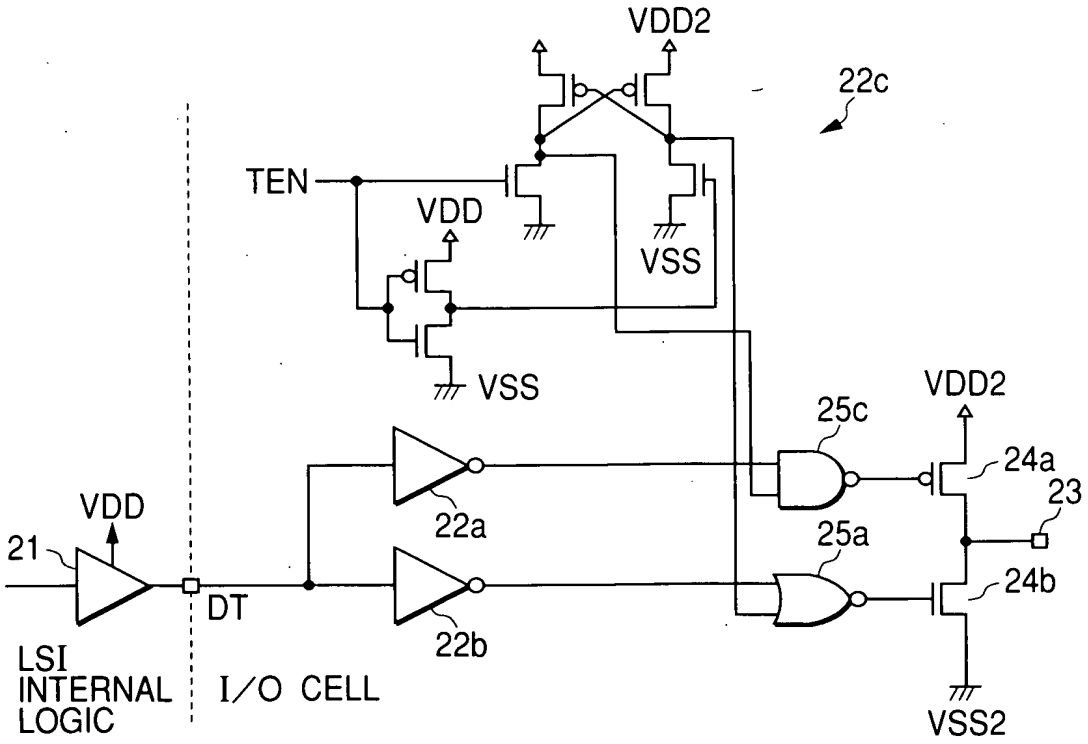

VDD2
22c
TEN
VDD
VSS
VSS
VDD2
25c
24a
23
VDD
21
22a
25a
24b
DT
22b
LSI
INTERNAL
LOGIC
I/O CELL
VSS2

FIG. 9

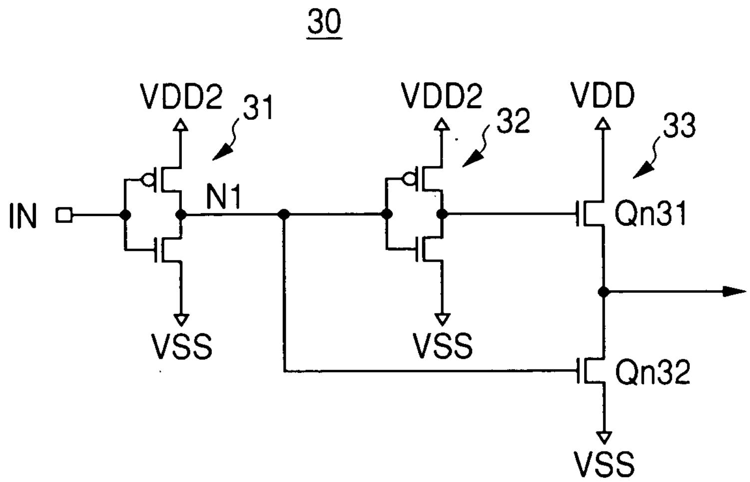

30
VDD2
31
VDD2
32
VDD
33
IN
N1
Qn31
VSS
VSS
Qn32
VSS

FIG. 10

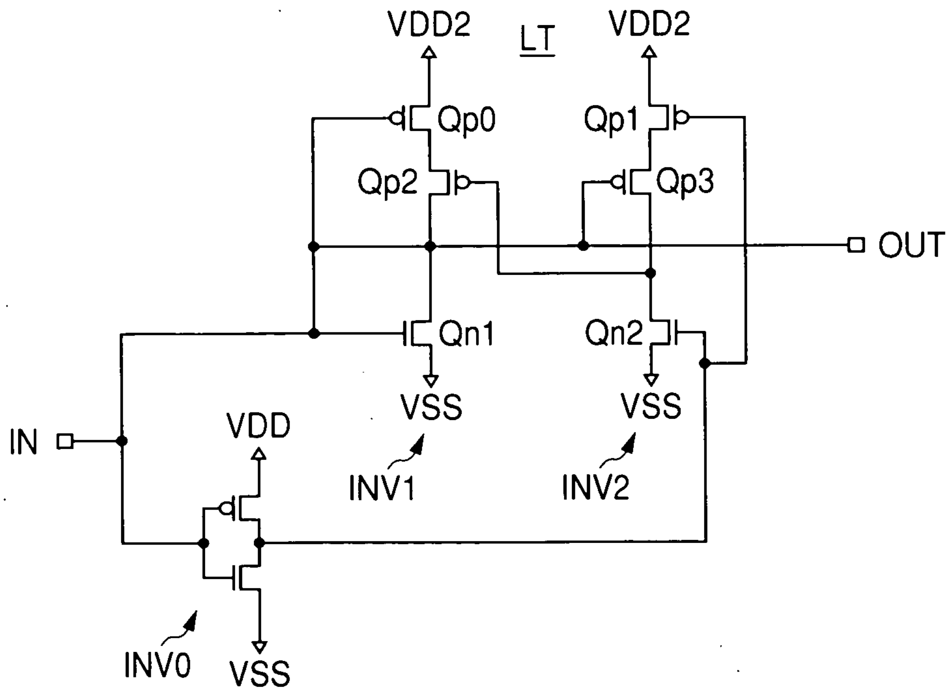

VDD2
LT
VDD2
Qp0
Qp1
Qp2
Qp3
OUT
Qn1
Qn2
VSS
VSS
IN
VDD
INV1
INV2
INV0
VSS

FIG. 11

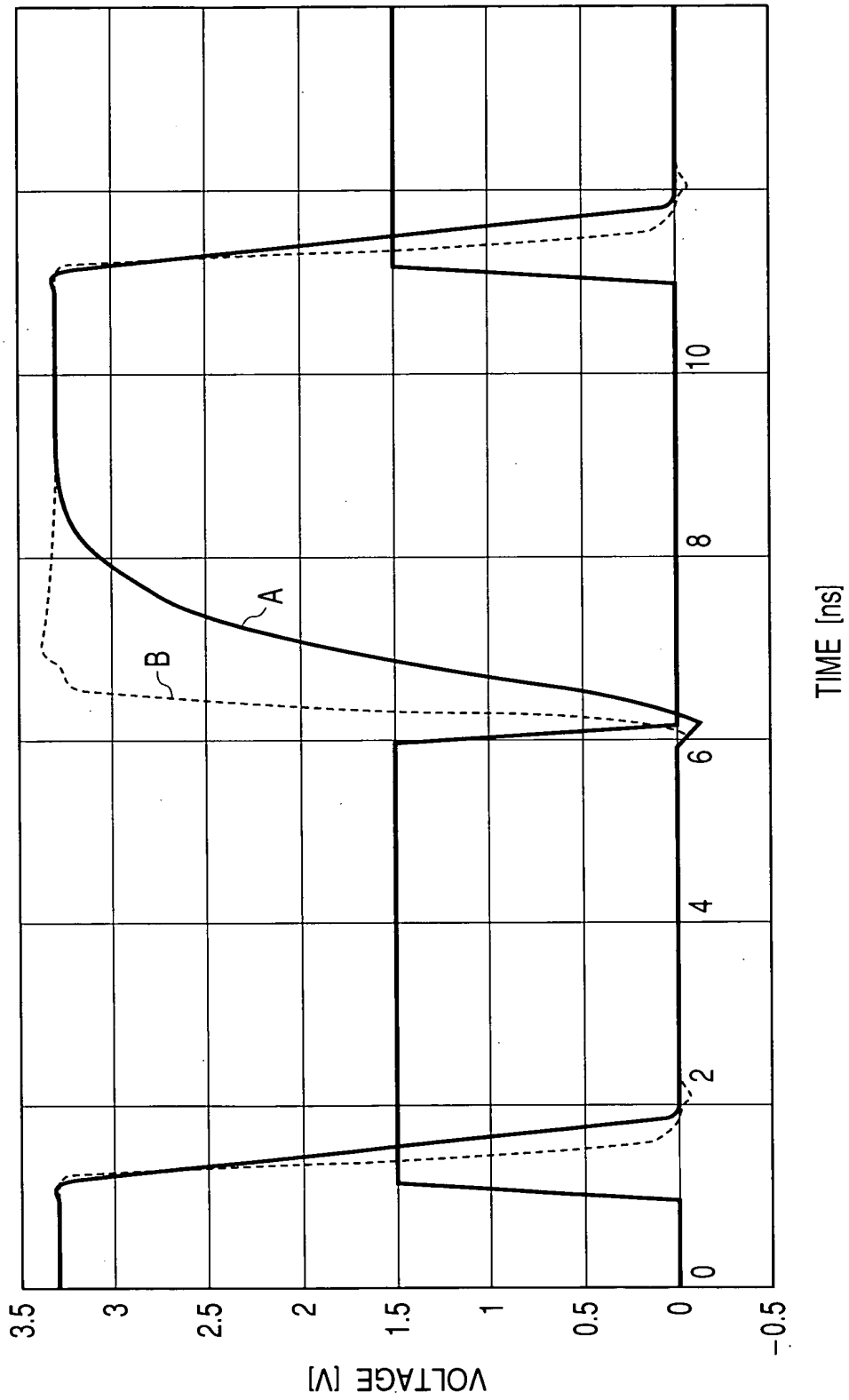


FIG. 12

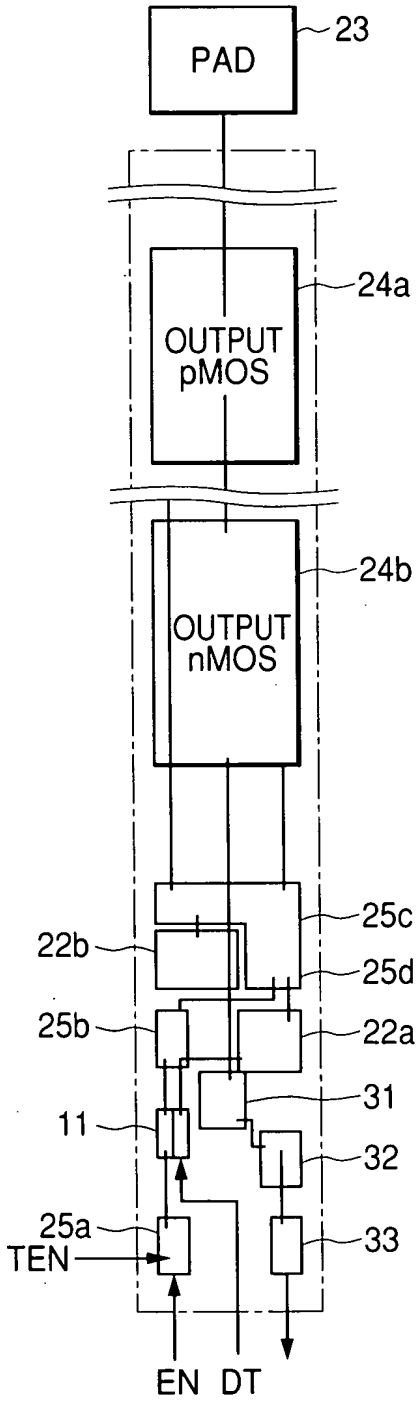


FIG. 13